Amendments to the Specification

On page 3, line 9, please delete the paragraph and insert the following:

--Addressing a particular cell is performed by applying a voltage to the appropriate word line and bit line. For example, to address cell 10, word line 20 and bit line 22 would have a voltage applied to them. These will be referred to as the active word line (AWL) and the active bit line (ABL). The other bit lines and word lines will be referred to as passive lines, PBLs and PWLs, respectively. The passive lines have a bias voltage applied to them to assure quiescent level electric fields across the cells. This prevents erroneous reads and writes.--

On page 3, line 26, please delete the paragraph and insert the following:

--The device control circuitry 28 may be one of several combinations of input and output multiplexers, row and column decoders, sense amplifiers, etc. In addition, this circuitry will receive and assert various control signals such as Serial Data In (SDI), Serial Data Out (SDO), a clock signal (CLK), and busy signal. The busy signal prevents the device from accepting any other control inputs during the assertion of that signal, usually when the memory array 24 is performing an internal read or write. These signals also give rise to other options in designing a memory system based upon the ferroelectric memories.—

On page 4, line 22, please delete the paragraph and insert the following:

--Most memory operations in current practice act on memory sectors, where a sector is 512 bytes. Using the above dimensions of the example memory device, W number of these devices would be linked together to form one memory sector, 512 x 8 bits/byte equals 4096 bits, which in turn equals Y bits x W device. These memory devices can be arranged sequentially, under the control of one system controller, such as that shown at 38. The system controller generates the BUS CNTRL and command CMD signals to handle bus transactions and communications with a system in which the memory system resides through a SYSTEM INTERFACE.—

On page 4, line 27, please delete the paragraph and insert the following:

--In a read sequence, address and control signals are sent to all devices simultaneously. In some embodiments data lines may also be common to all of the devices to conserver routing on the printed circuit board (PCB). During the first part of the read sequence, as will be discussed in more detail later, the individual devices assert the BUSY signal. When the first device in the sequence deasserts the BUSY signal, the system controller 38 generates a serial data out signal SDO, used as the input of the first of the sequentially arranged memory devices. Any number memory devices may be used, defined as the variable W above. However, at least two memory devices must be present to perform the sequential linking discussed here. An extension of the signal names will be used in the following figures to indicate from which device a signal comes, such as serial data out signal for the first memory device would be referred to as SDO-1.--

On page 6, line 5, please delete the paragraph and insert the following:

--A half cycle prior to the clock cycle, N, on the falling edge of the clock signal, CLK, the controller transitions related to read cycle occur. The controller asserts the high addresses, HA on the address bus 40 in Figure 4. LA will refer to low addresses. The controller also asserts the RD and ENB signals, and IGRD signal, if desired. With RD asserted low, the system assumes that this is a read cycle. The controller also asserts the address strobe, ADS, at this time.--

On page 6, line 32, please delete the paragraph and insert the following:

--During the period M-1 to M-0.5, the memory device assumes a wait state until the controller asserts the SDI signal on the memory device. The controller is actually requesting that the serial data be read out, but is used to initiate the SDI sequence for the memory chips. A half clock cycle later, at M, the memory chip recognizes the assertion of the SDI signal and drives high data <255:224> onto the data bus on the rising

edge. In the timing diagram, the high data is referred to as HD7. In the subsequent memory cycles, M+1 through M+7, the memory chip drives the corresponding data onto the data bus. The data corresponds to the clock cycles as follows: M+1 is low data, LD6, <223:192>; M+2 is HD5 <191:160>; M+3 is LD4 <159:128>; M+4 is HD3 <127:96>; M+5 is LD2 <95:64>; M+6 is HD1 <63:32>; and M+7 is <31:0> is LD0. However, the order of the data out on the data bus is flexible.--